

OTF
JUN 16 2005
PATENT & TRADEMARK OFFICE
JC98

FIG. 1

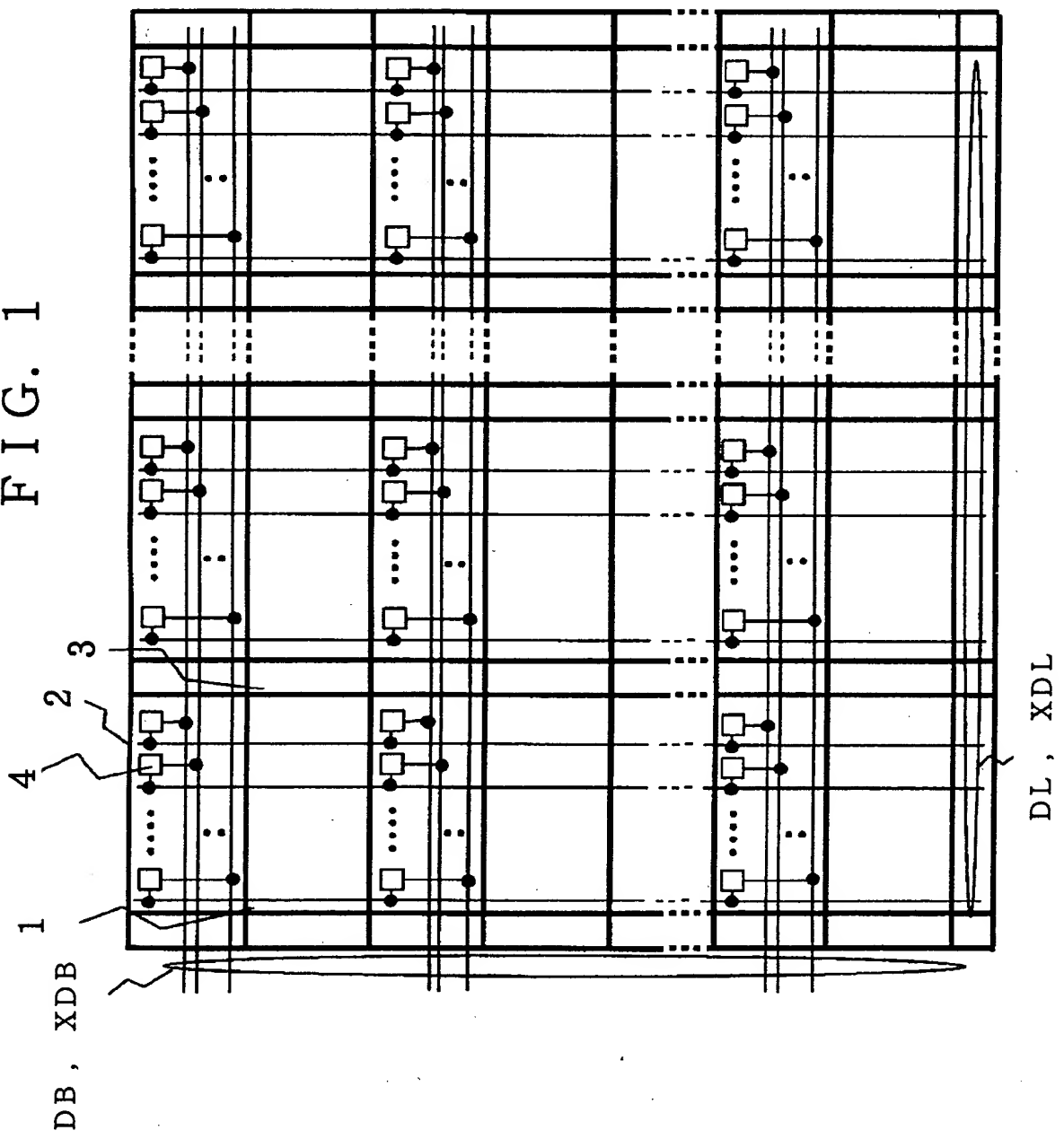
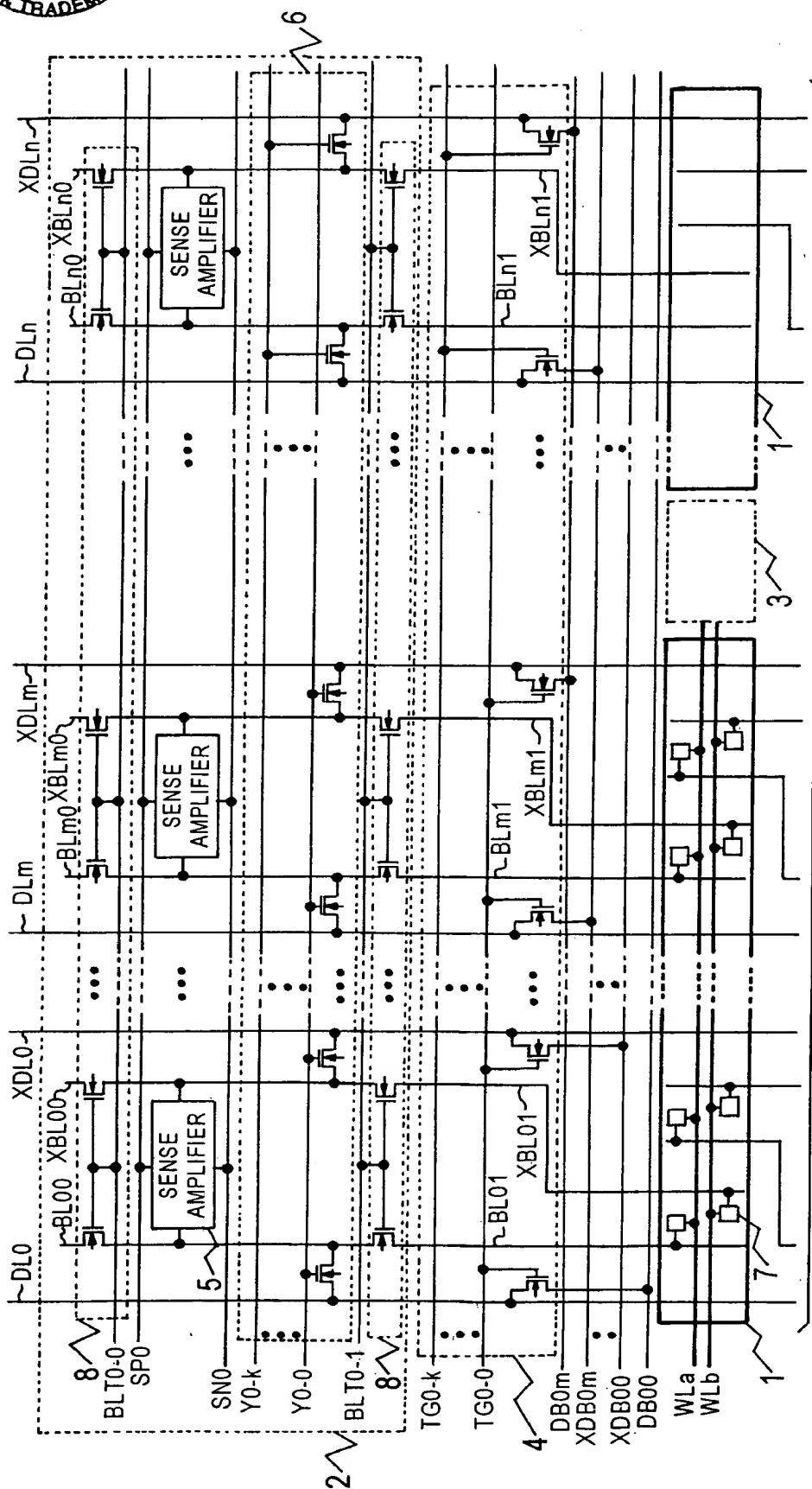


FIG. 2A



Continue on Fig. 2B



REPLACEMENT SHEET

FIG. 2B

Continue on Fig. 2A

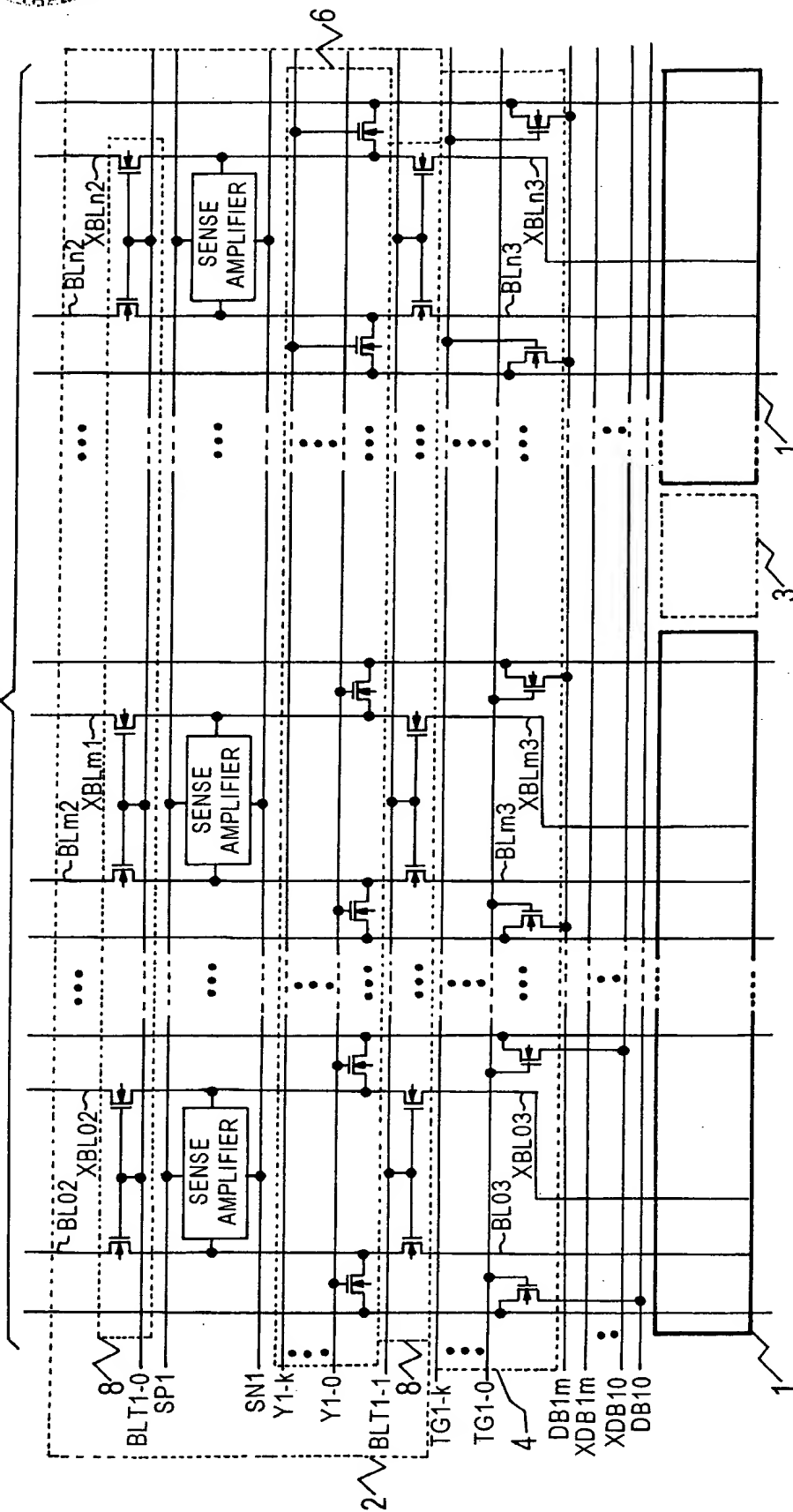


FIG. 3

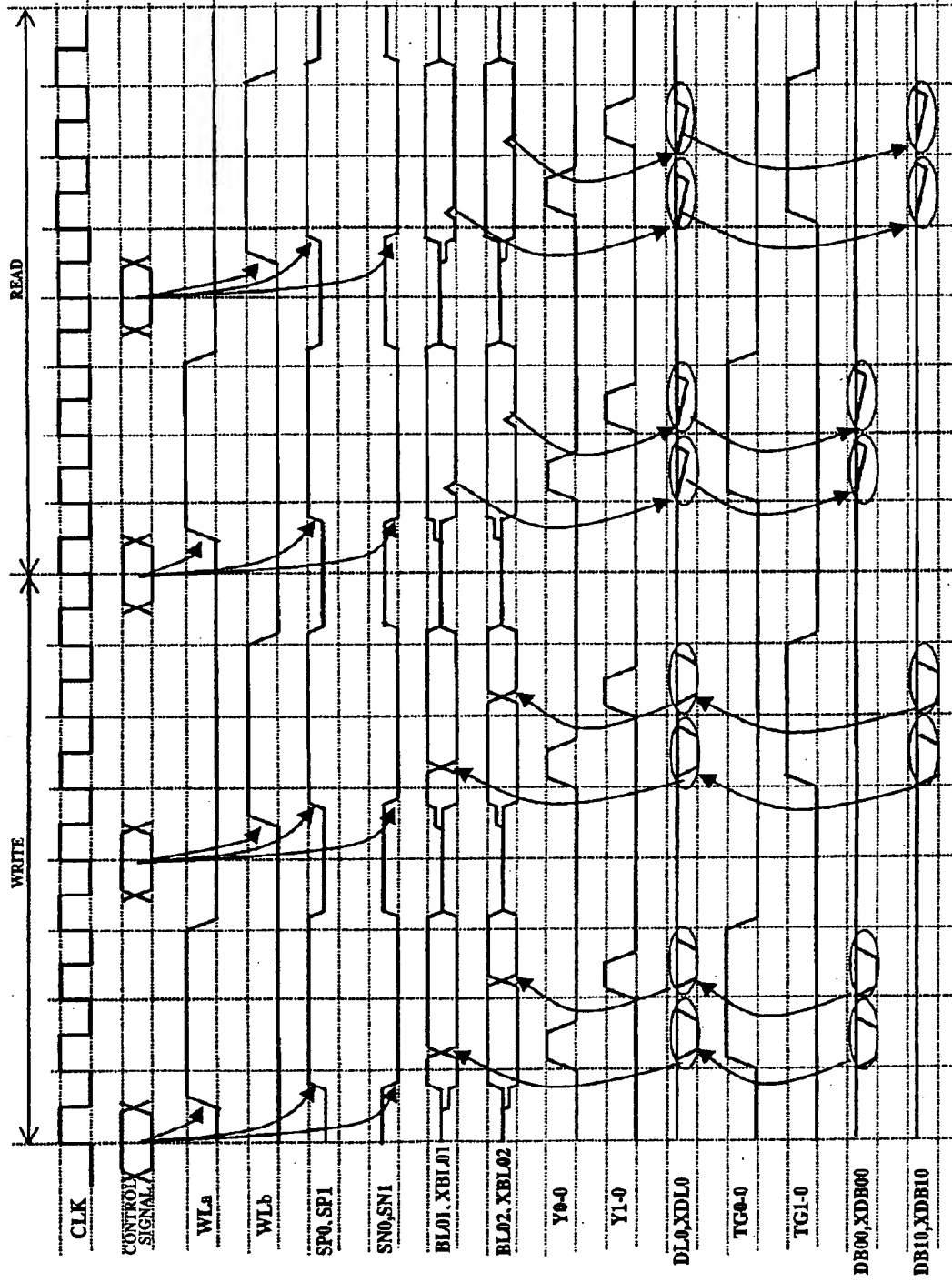
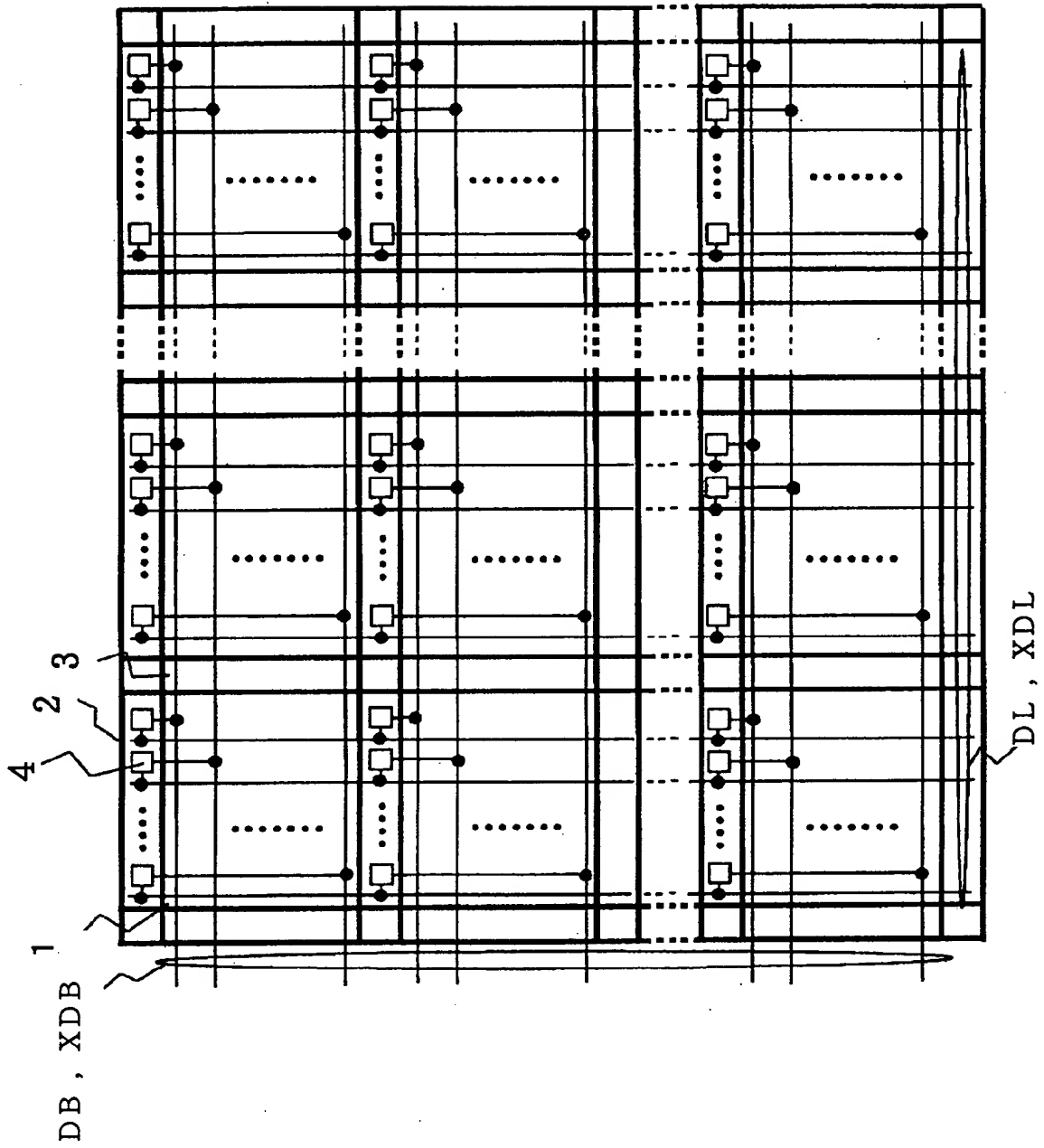


FIG. 4





The diagram illustrates a memory array structure with multiple rows and columns. The rows are labeled on the left as DL0, DLm, and DLn, with ellipses indicating intermediate rows. The columns are labeled at the bottom as BLT0-0, SP0, SN0, Y0-k, Y0-0, BLT0-1, TG0-k, TG0-0, DB0m, XDB0m, WL a, WL b, XDB00, and DB00, with ellipses indicating intermediate columns. The array is divided into three main sections by dashed lines, labeled 1, 3, and 5. Each section contains a sense amplifier (labeled SENSE AMPLIFIER) connected to a pair of bit lines (BLm0, XBLm0) and a pair of word lines (WL a, WL b). The sense amplifiers are connected to the bit lines via access transistors (represented by small squares). The word lines are connected to the access transistors via access transistors (represented by small squares). The diagram also shows various other components such as capacitors, transistors, and interconnects, all arranged in a grid-like pattern. A legend at the bottom right identifies the symbols for the access transistors and the sense amplifiers.

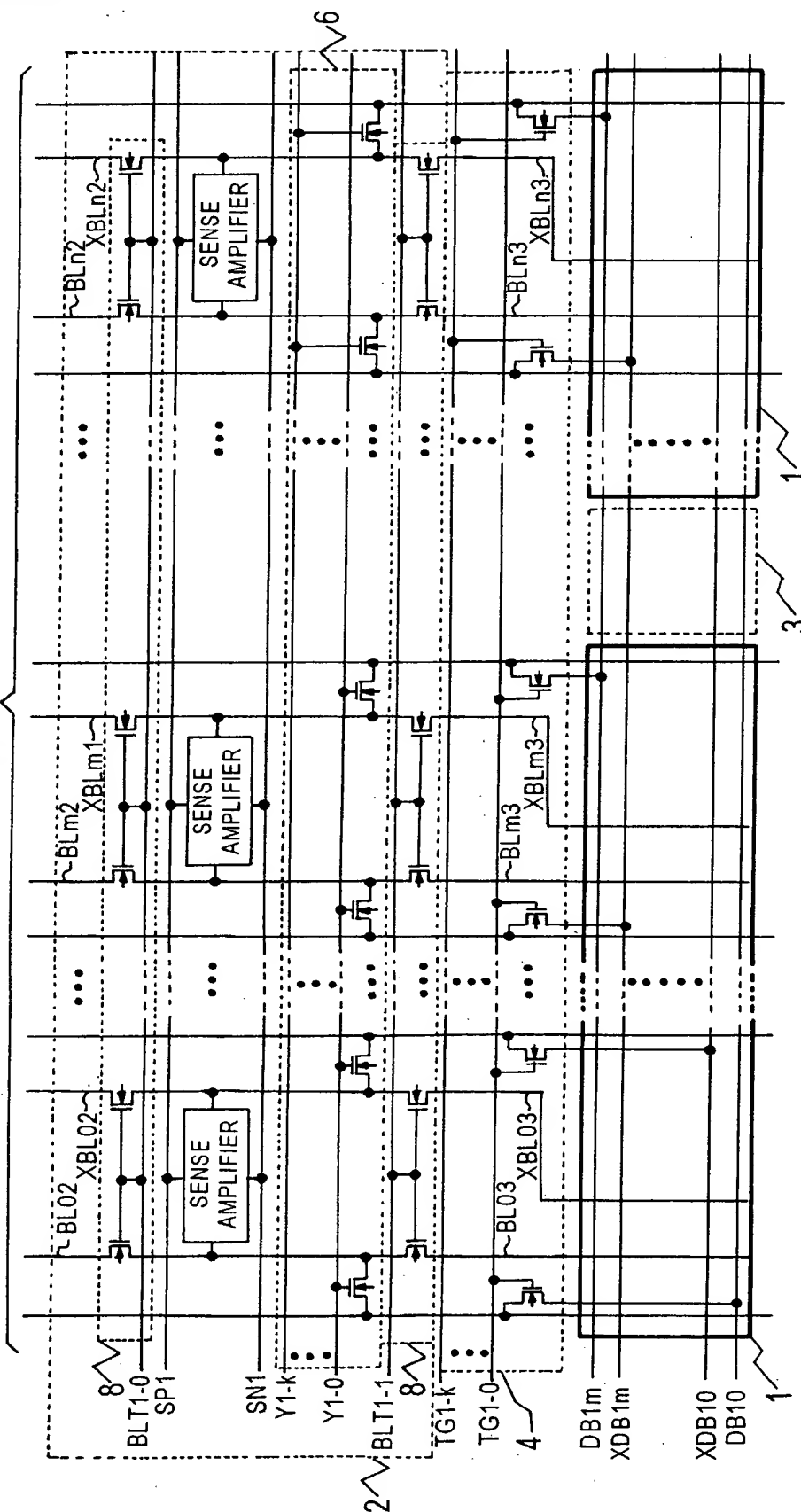
Continue on Fig. 5B



REPLACEMENT SHEET

FIG. 5B

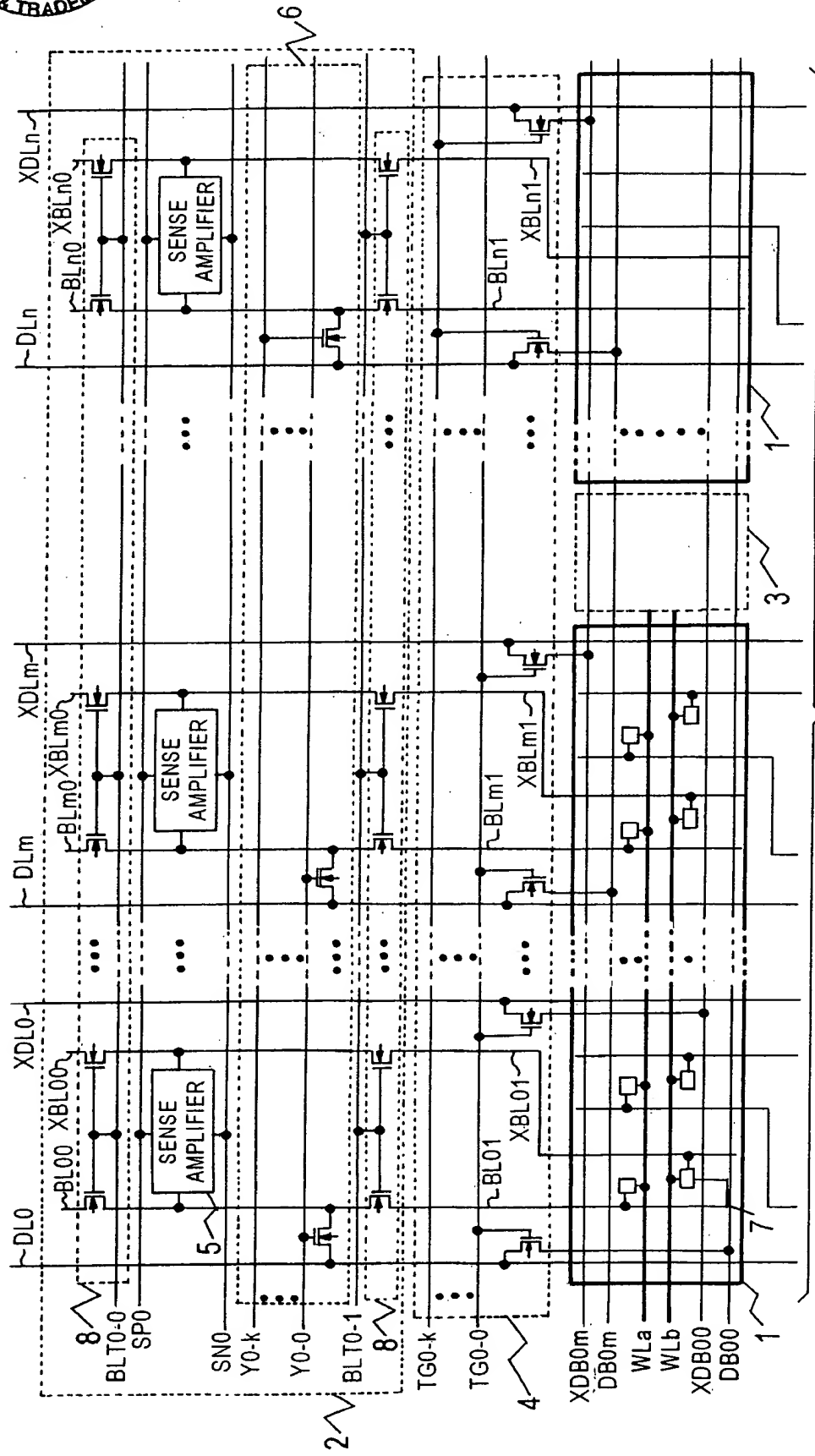
Continue on Fig. 5A





REPLACEMENT SHEET

FIG. 6A



Continue on Fig. 6B

FIG. 6B

Continue on Fig. 6A

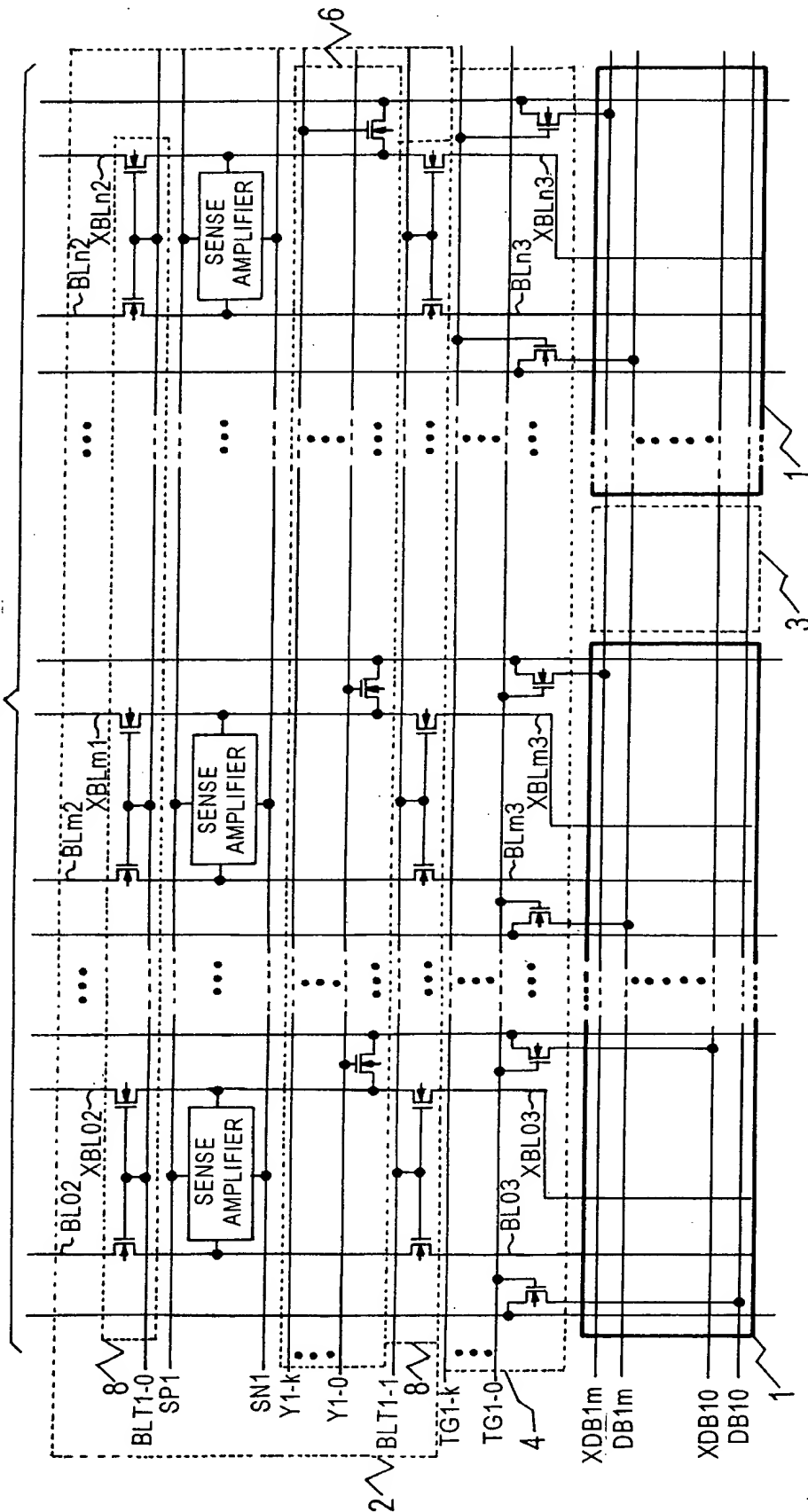


FIG. 7

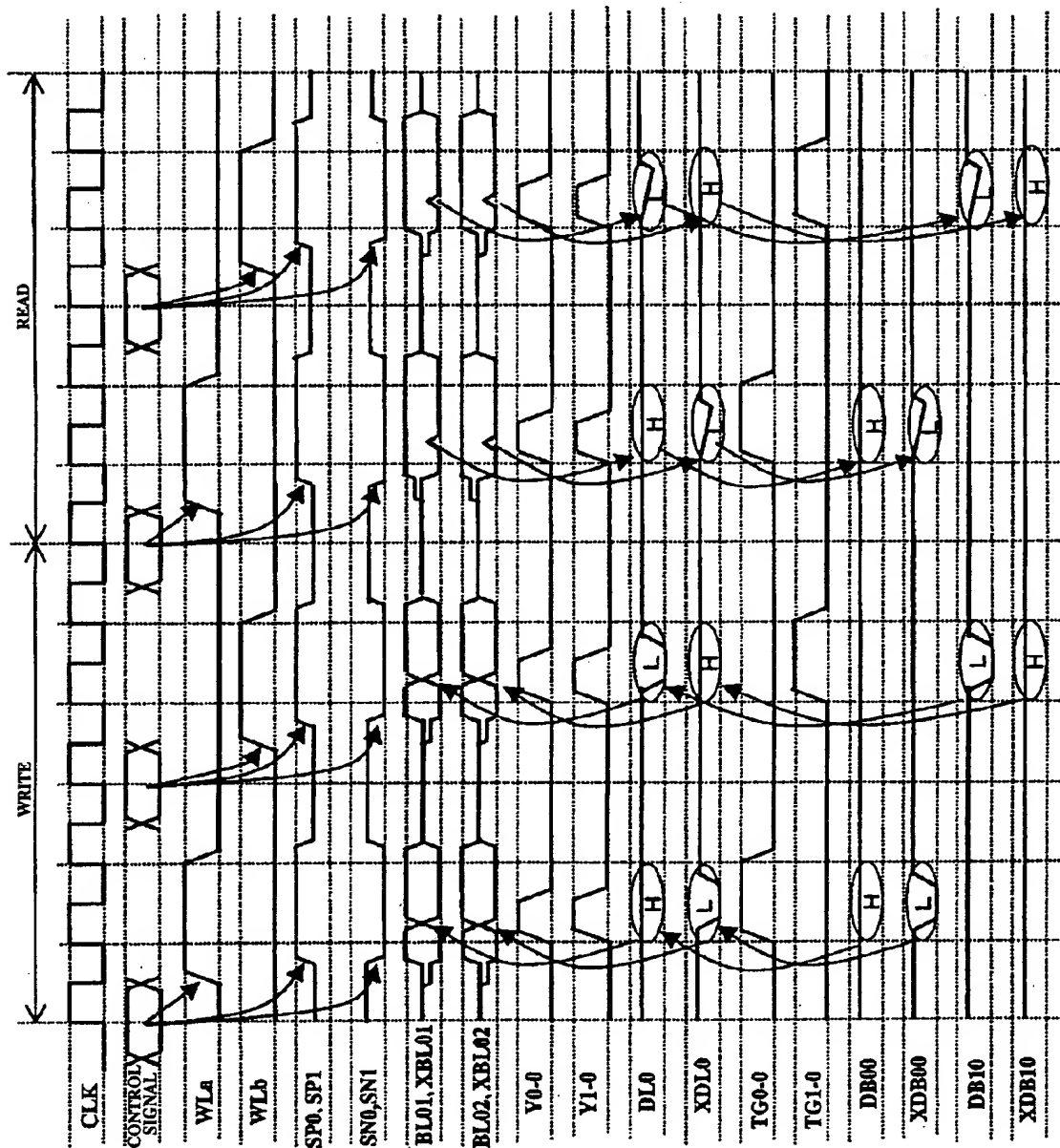
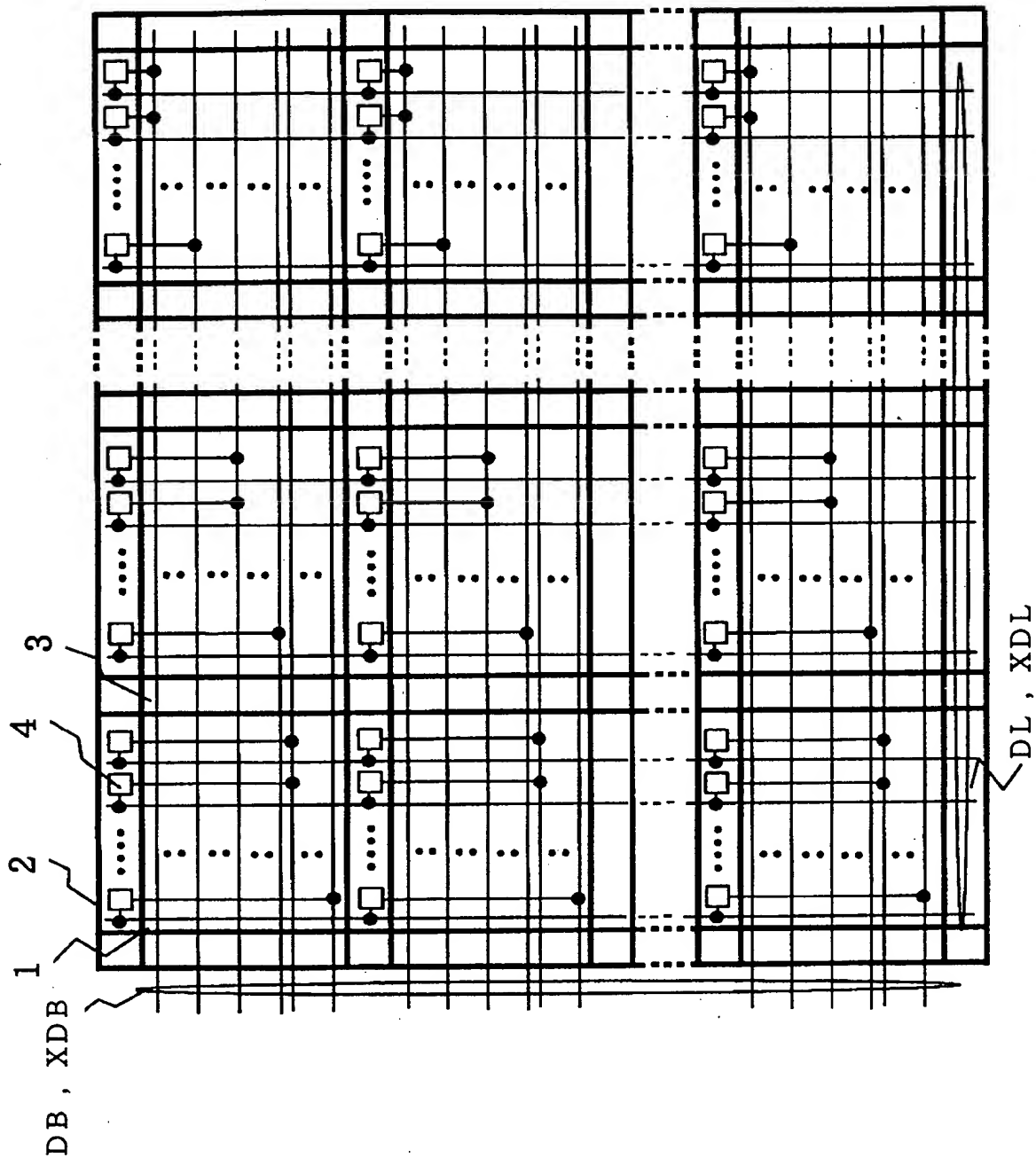


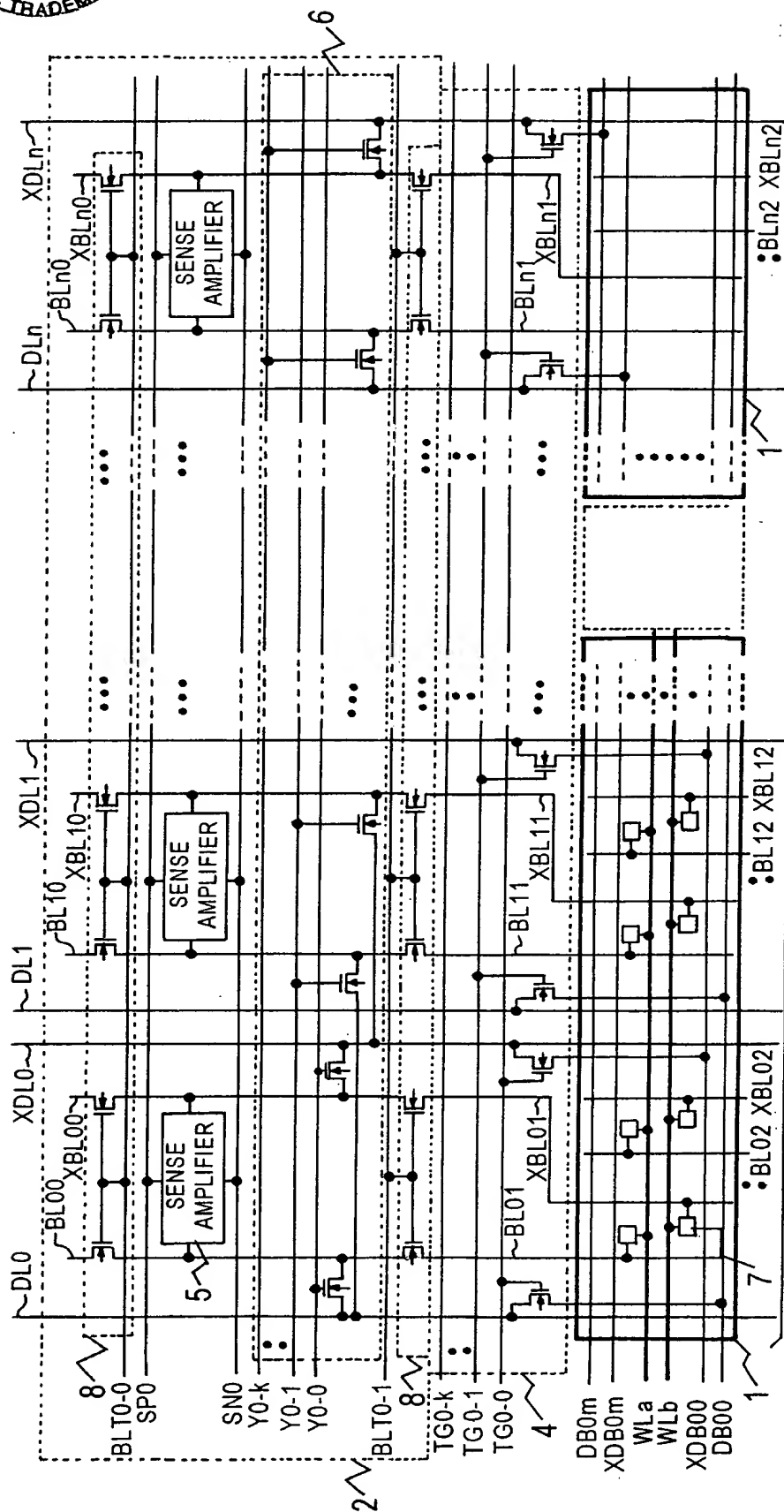
FIG. 8





REPLACEMENT SHEET

FIG. 9A



Continue on Fig. 9B

FIG. 9B

Continue on Fig. 9A

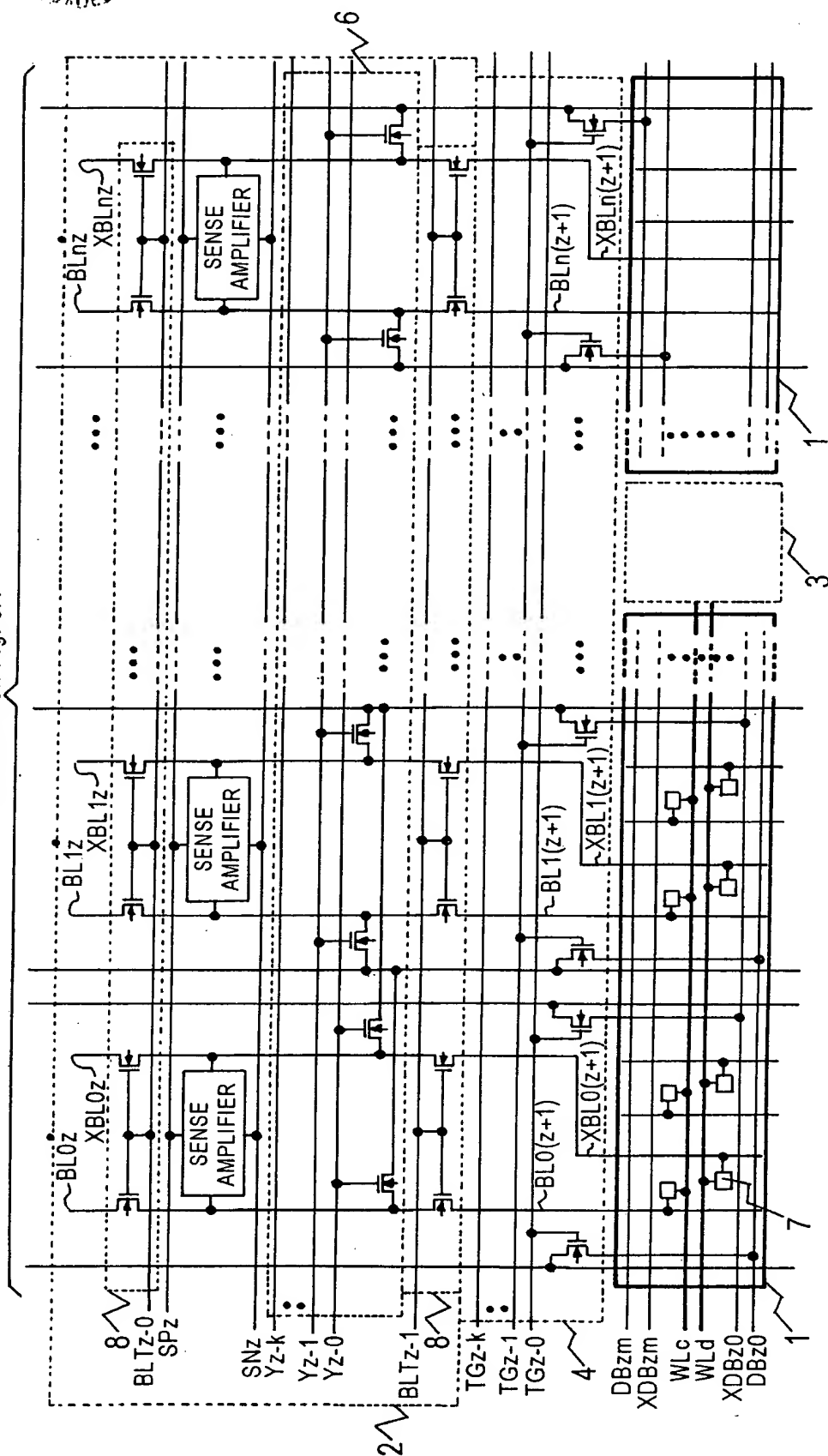


FIG. 10

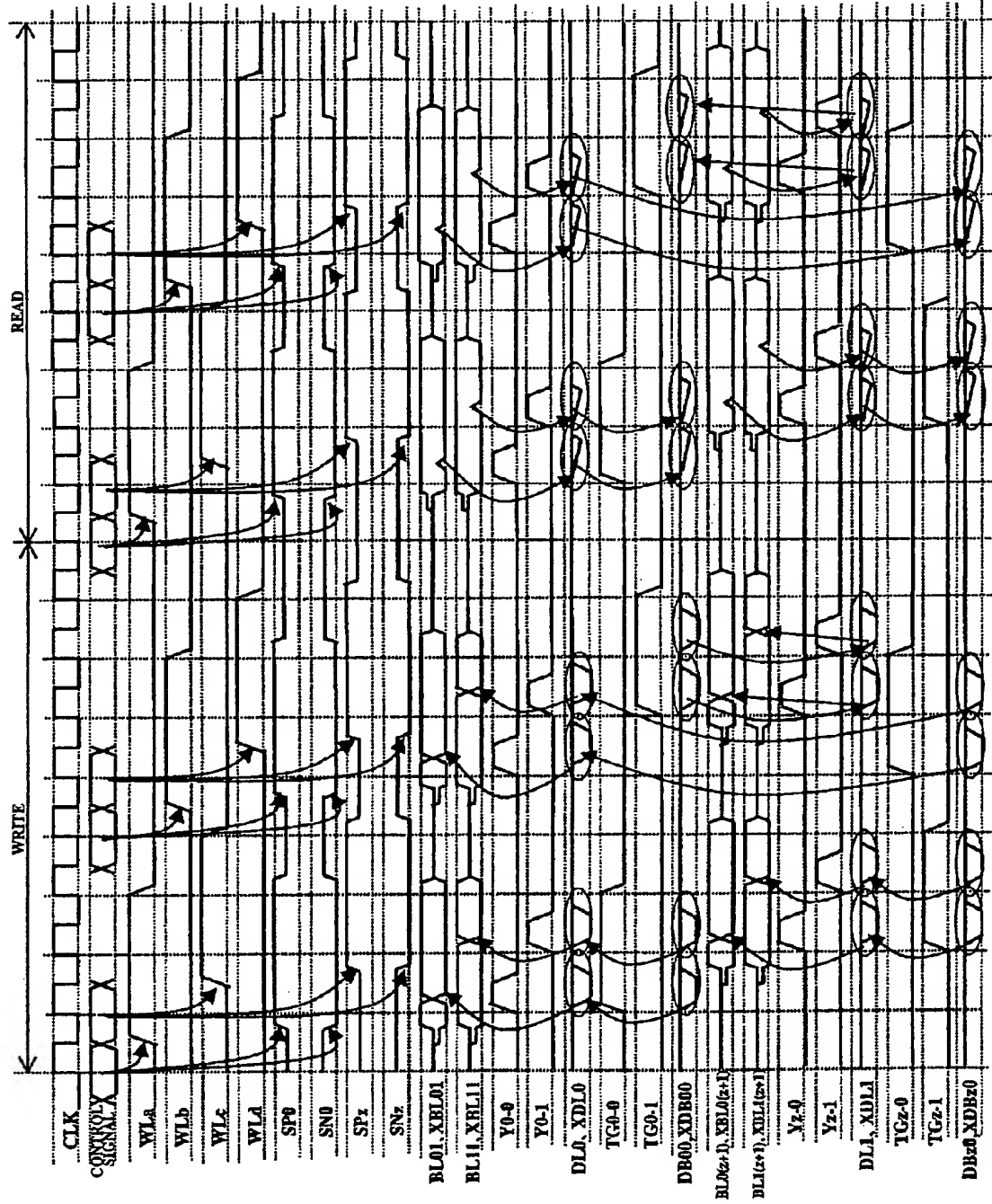


FIG. 11

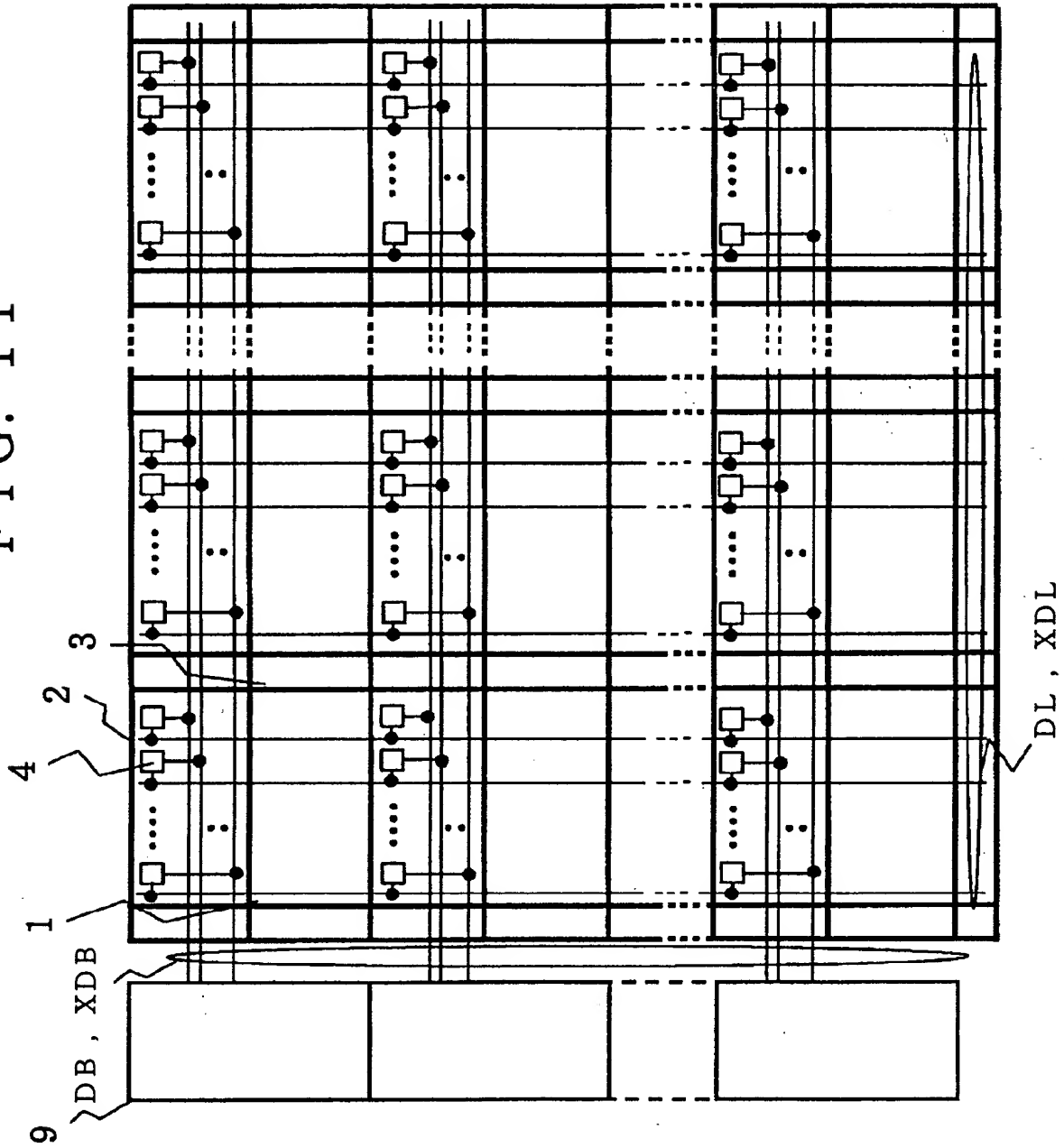


FIG. 12

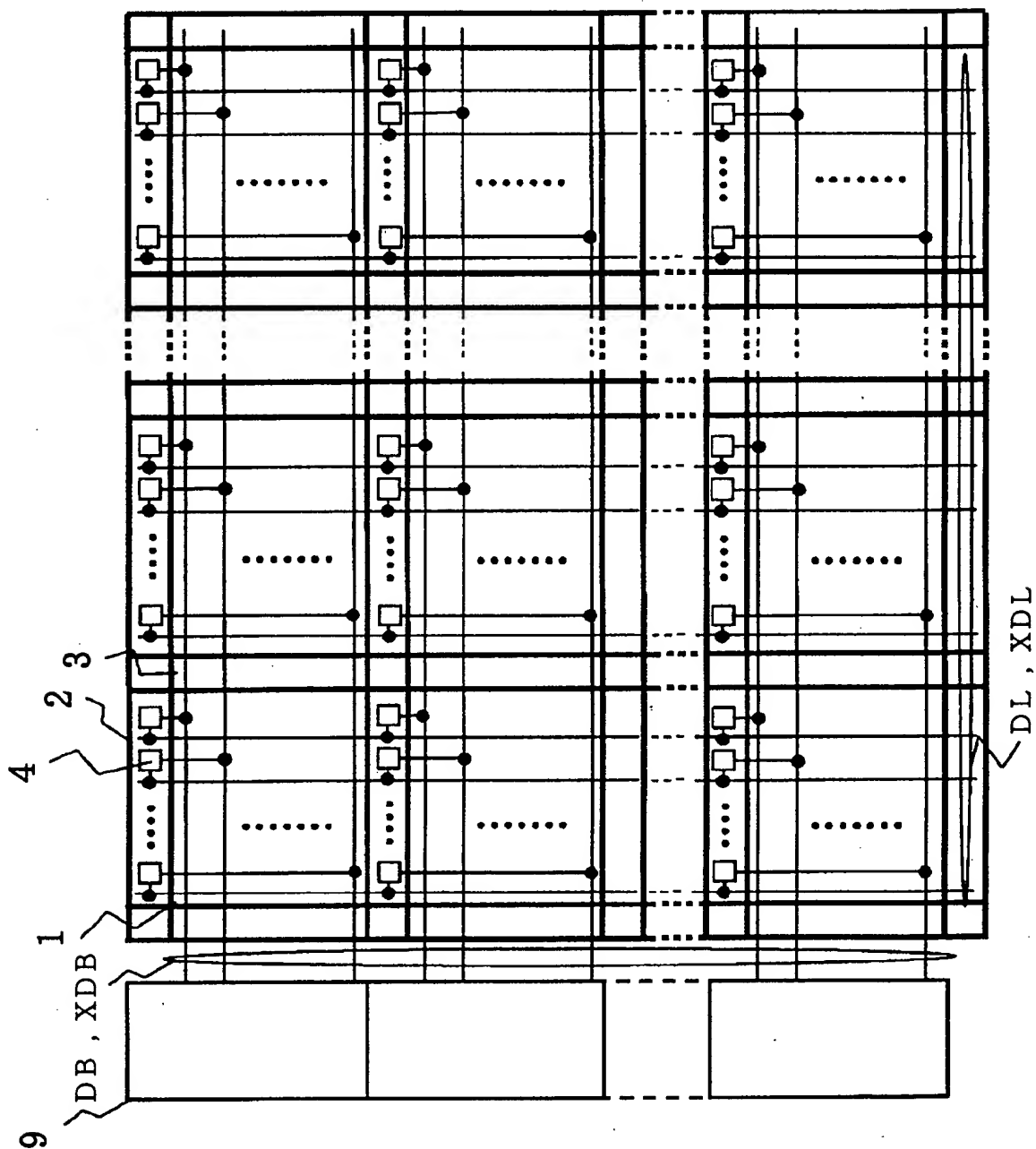


FIG. 13

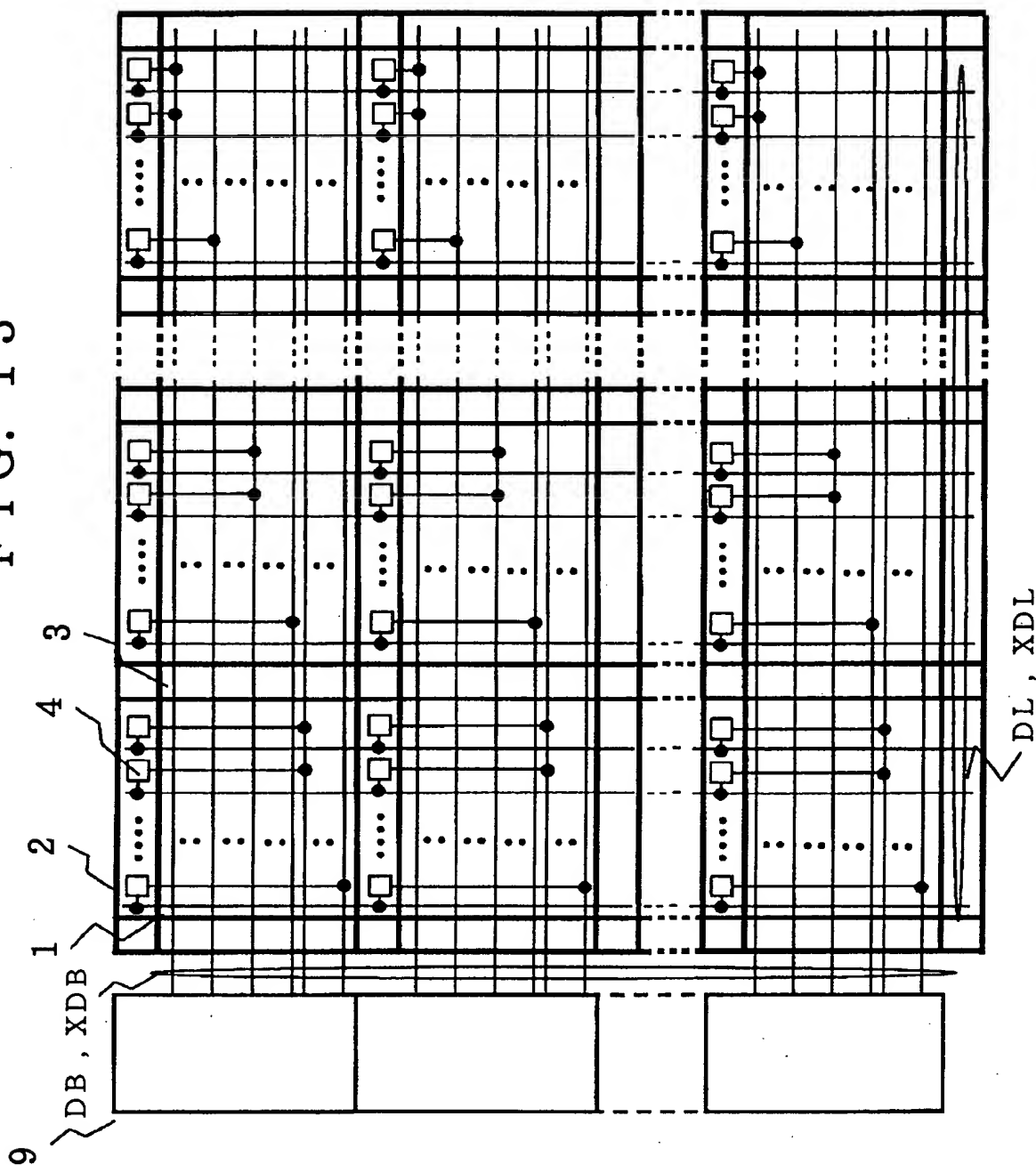




FIG. 14

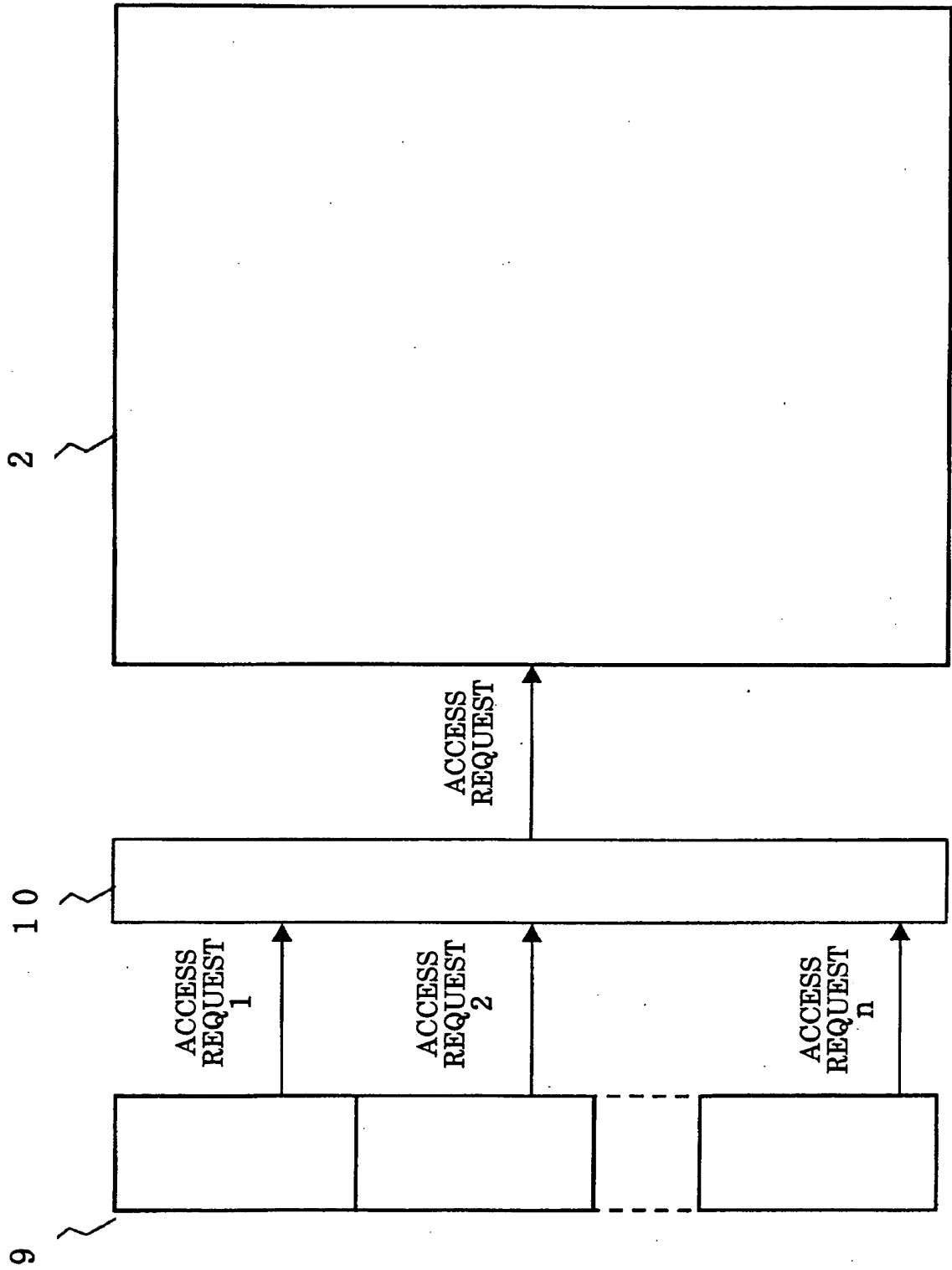
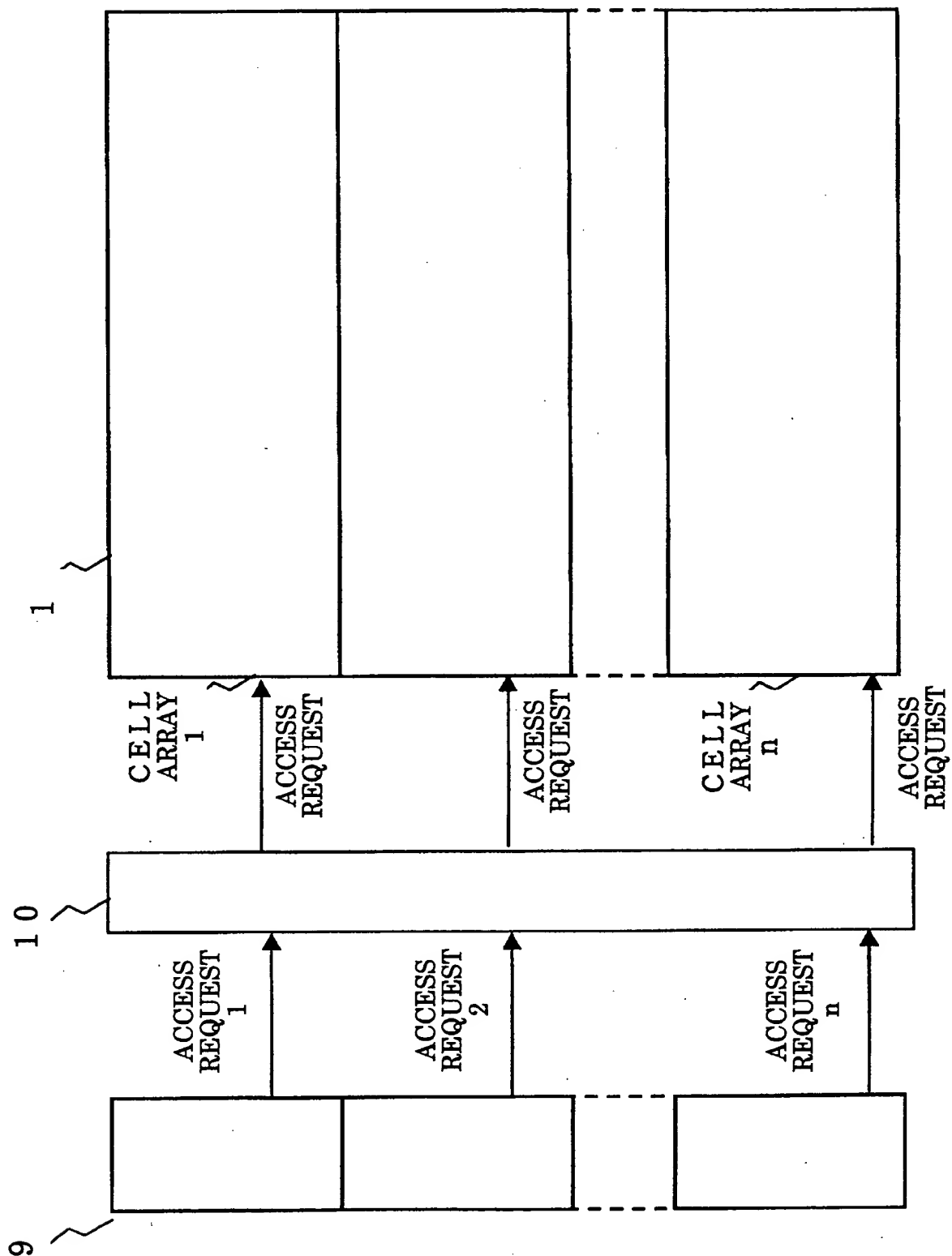


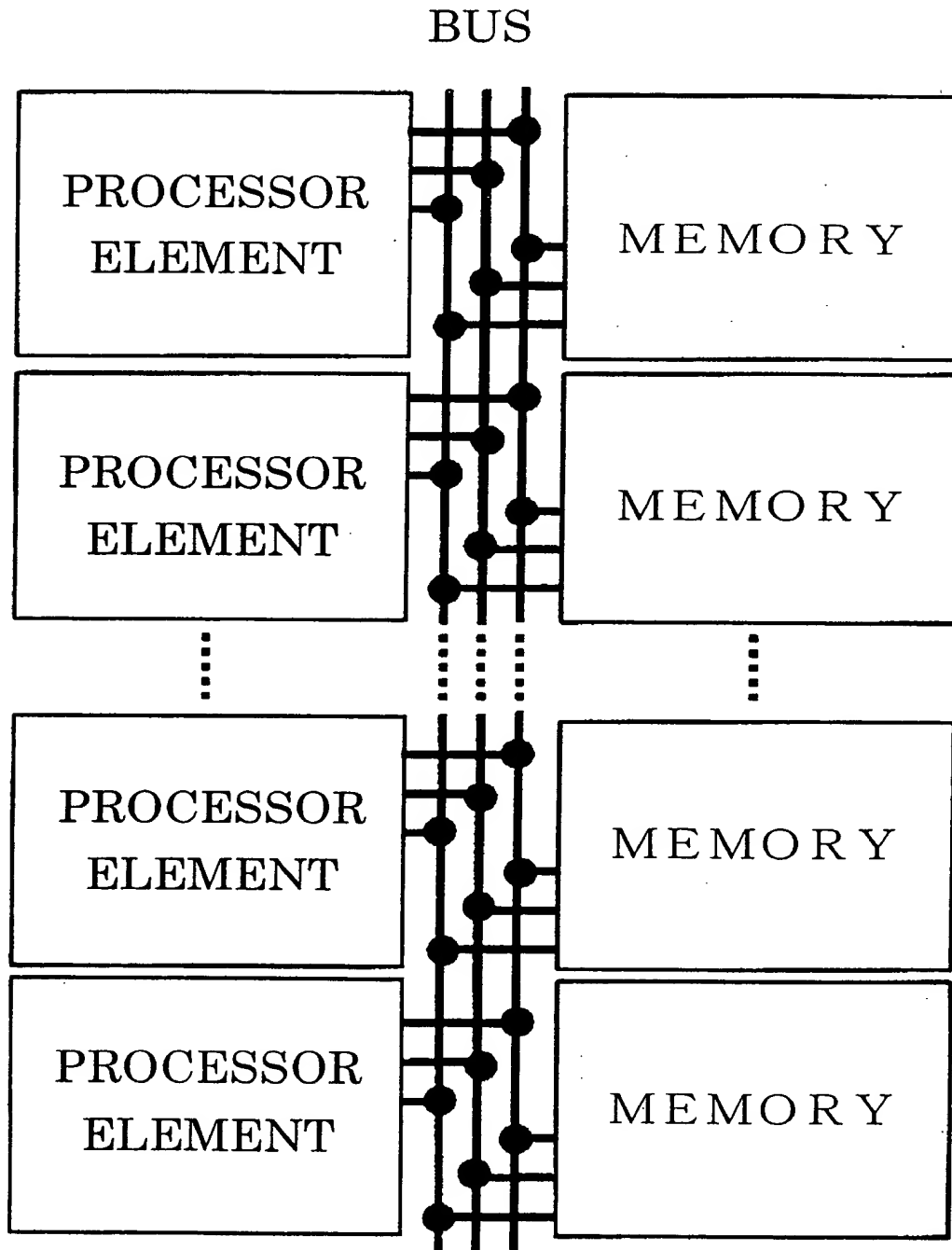
FIG. 15





REPLACEMENT SHEET

FIG. 16
PRIOR ART





Replacement Sheet

FIG. 17

PRIOR ART

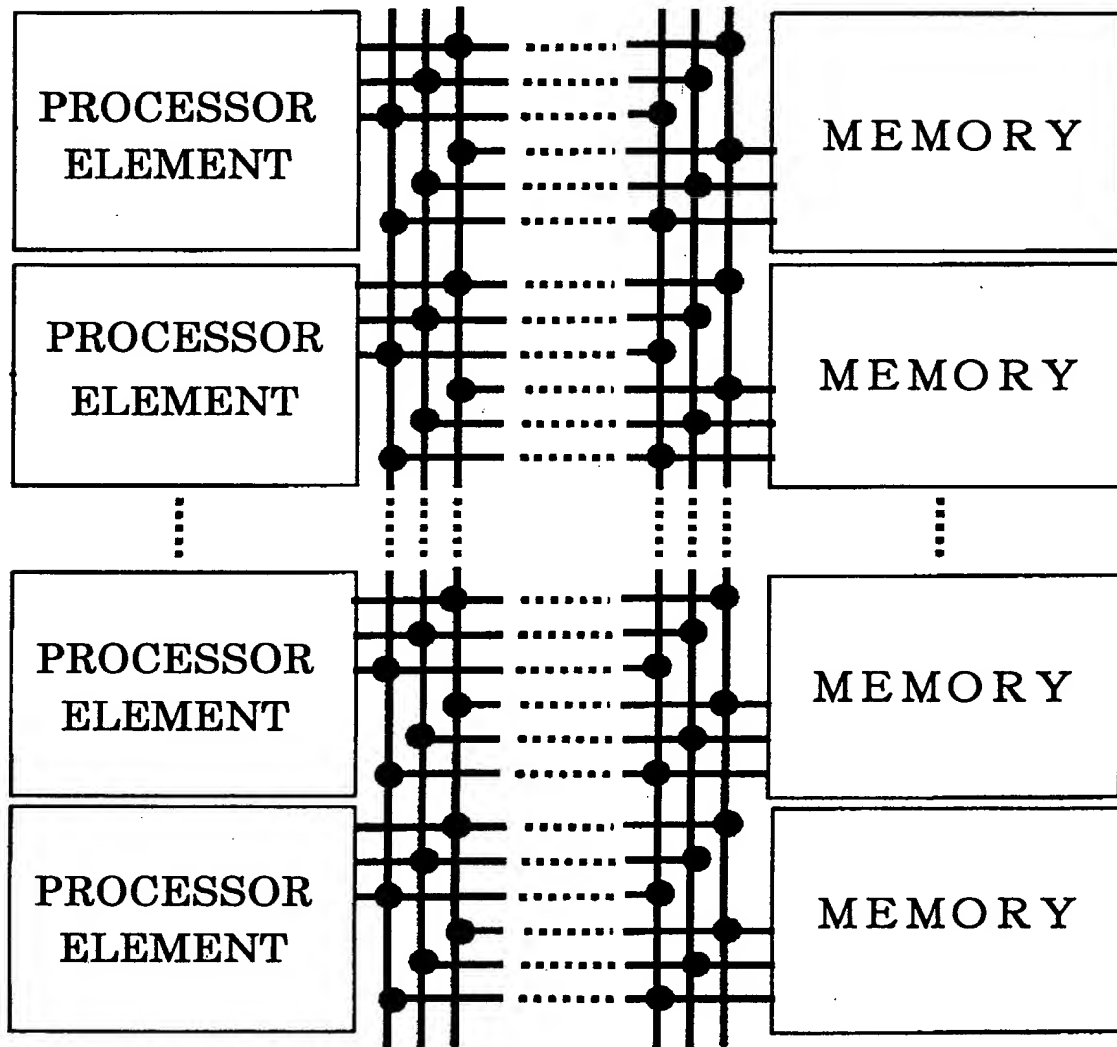




FIG. 18
PRIOR ART

